Low-Loss 2- and 4-bit TTD MEMS Phase Shifters Based on SP4T Switches

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***Abstract*—2- and 4-bit microelectromechanical system (MEMS) X- to K_u-band true-time-delay phase shifters with a very low insertion loss are described. The phase shifters are fabricated on 200-μm GaAs substrates and the low loss is achieved using MEMS SP4T switches, which reduce the number of switches in the signal path by half when compared to conventional designs with SP2T switches. Measurements indicate an insertion loss of -0.6 ± 0.3 and -1.2 ± 0.5 dB at 10 GHz for the 2- and 4-bit designs, respectively. The measured losses agreed very well with Momentum simulations and are the lowest reported to date. The 2-bit phase shifter performed well from dc–18 GHz, with -0.8 ± 0.3-dB insertion loss at 18 GHz and a return loss of < -10.5 dB over dc–18 GHz.**

***Index Terms*—Microelectromechanical system (MEMS) devices, phase shifters, radar antennas, radar receivers.**

I. Introduction

PHASE shifters are critical components in the electronic steering of antenna beams in phased-array antennas. Such electronically scanned arrays (ESAs) may be the active or passive types [1]. In the active phased array, a transmit/receive (T/R) module containing a power amplifier and a low-noise amplifier (LNA) is placed directly behind each radiating element. The phase shifter is placed after the T/R module and, therefore, both the transmit power and noise figure are unaffected by the phase-shifter loss. However, due to the high component count, the active phased array is very costly and bulky, especially when a very large system is required, such as those for space applications. In the passive phased array, each T/R module usually feeds several phase shifters, which are each placed directly behind the radiating element, thus directly contributing to the noise figure of the system. The transmit power is also directly reduced by the loss of the phase shifters. The advantage is that a simpler and lower cost system results due to the smaller number of T/R modules and other components required. However, this is feasible only if the phase shifters are of very low loss since the T/R modules must compensate for the loss in the phase shifters. A high loss in the phase shifters means that the T/R module needs to be much higher in transmit power, larger in size, and more costly, thus defeating the purpose of achieving a simplified design with a passive array.

Conventional wide-band digital true-time-delay phase shifters are mostly built using SP2T switches made of p-i-n diodes, MESFETs, or high electron-mobility transistors (HEMTs) and the insertion loss is usually in the range of -4 to -6 dB at X-band for a 4-bit design [3], [4], limited by the losses of semiconductor switches used in a multibit phase-shifter implementation. With the advent of RF microelectromechanical system (MEMS) switches, these phase shifters have been redesigned recently using low-loss dc-contact or capacitive MEMS shunt or series switches [2], [5]–[7] and the losses have been greatly reduced (-1.5 to -2.0 dB for 4-bit designs). However, the size of the lowest loss MEMS phase shifter to date remains large (50 mm^2 for a 2-bit design and 100 mm^2 for a 4-bit design), and the loss of the smallest 4-bit MEMS phase shifter is more than -2 dB at 10 GHz [2], [5].

This paper presents novel 2- and 4-bit phase shifters, which achieve both the lowest loss and smallest size in MEMS phase shifters reported to date. Although the phase shifters are optimized for X-band operation, the 2-bit design performs well from dc–18 GHz and the 4-bit design from dc–16 GHz. This performance level is achieved using SP4T switches designed with MEMS series switches, which reduces the number of switches in any signal path by half (Fig. 1). The MEMS switch used is a series dc-contact switch from Rockwell Scientific, Thousand Oaks, CA, which has a very low up-state capacitance of 1.75 fF and an R_s of 1–2 Ω [8]. Such an approach using SP4T switches in switched-line phase shifters is very difficult with semiconductor devices (especially if wide bandwidth is desired) because of the much higher off-state capacitances associated with the GaAs p-i-n diode or FET switches, which results in off-path resonances that greatly reduce the bandwidth [9]. In contrast, the very low up-state capacitance of series MEMS switches ensures phase-shifter designs with a very wide bandwidth.

II. SP4T Switch Modeling and Design

A. Equivalent Circuit of the MEMS SP4T Switch

Fig. 2 shows the layout of the MEMS SP4T switch. Since only one switch in each SP4T is activated to the down-state position at any time, the equivalent circuit with ideal switches ($R_s = 0\,\Omega, C_u = 0$ fF) consists of three "open" stubs connected between the input transmission-line section and an output section with a down-state series switch [see Fig. 3(a)]. Since the relatively short "open" stubs are capacitive in nature, both the input transmission line and the transmission line connected to

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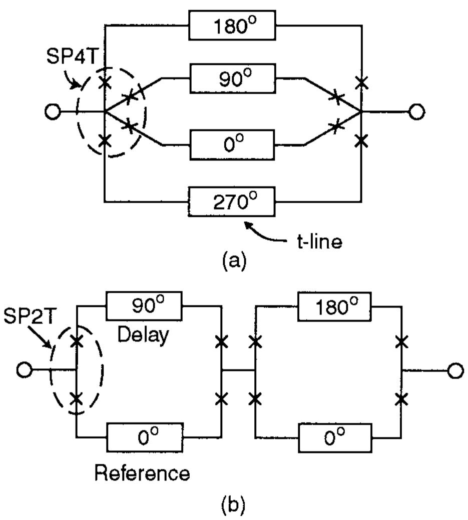

Fig. 1. Switched-line phase shifter based on: (a) SP4T and (b) SP2T switches.

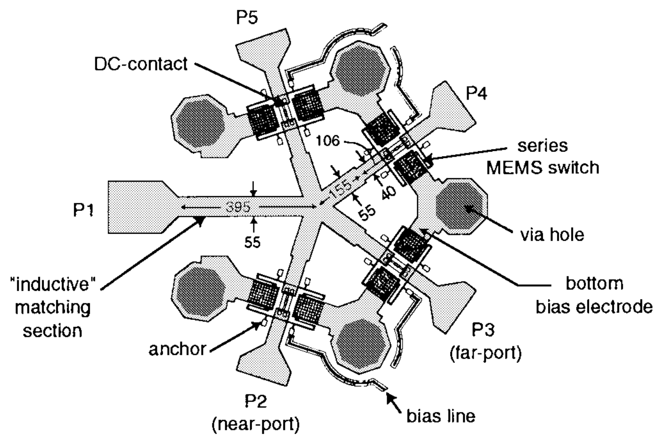

Fig. 2. Layout of SP4T switch.

the switch have to be of relatively high impedance (“inductive”) to form a “T-match” circuit for good input and output match.

A lumped equivalent model is obtained by replacing the inductive sections with a shunt-C, series-L π-equivalent circuit, and the open stubs with a shunt *R*-*C* circuits. The lumped model clearly illustrates the fact that the SP4T can be viewed as a “T-match” circuit, with two series L and a shunt $C(= C_1 + C_2 + C_3$ and ignoring the smaller capacitances). A wide-band match is obtained by changing the width and lengths of the five inductive sections to adjust the L and C values. The complete circuit model is shown in Fig. 3(b), where the MEMS switches are modeled using a simple capacitor $C_u = 2$ fF in the up-state and a resistor $R_s = 1\ \Omega$ in the down-state position.

The series-L, shunt-C configuration means that the insertion loss of the SP4T switch exhibits a “low-pass” characteristic, the “cutoff” frequency depending on the value of C (i.e., the length of the open stubs). In order to achieve the widest bandwidth, it is, therefore, important to decrease the length of the stubs by packing the switches as close as possible without causing problems in switch fabrication. With the layout in Fig. 2, the electrical length of each stub is only 5° at 10 GHz and the equivalent capacitance is 20 fF ($-j800\ \Omega$ at 10 GHz). This is relatively small and the SP4T switch maintains an impedance match up to around 20 GHz.

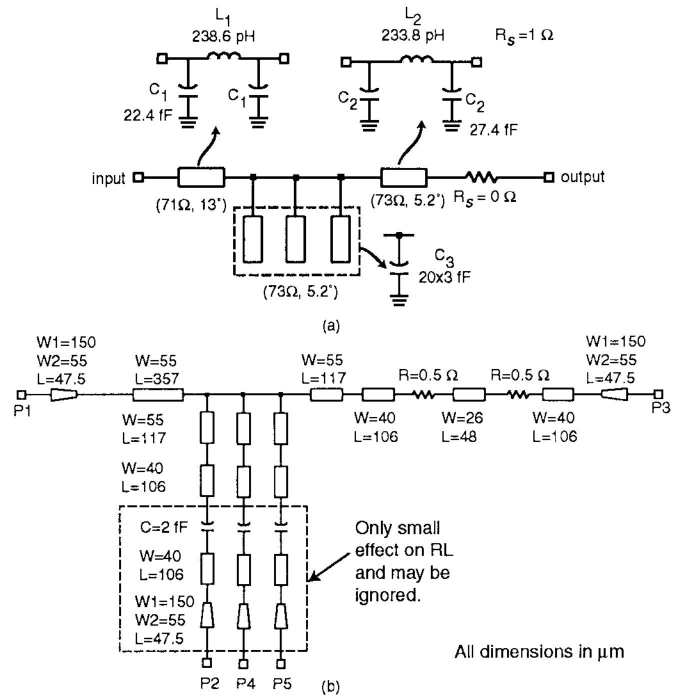

Fig. 3. Equivalent circuits of SP4T switch. (a) Ideal equivalent circuit at 10 GHz ($R_s = 0\ \Omega, C_u = 0$ fF). (b) Complete transmission-line model.

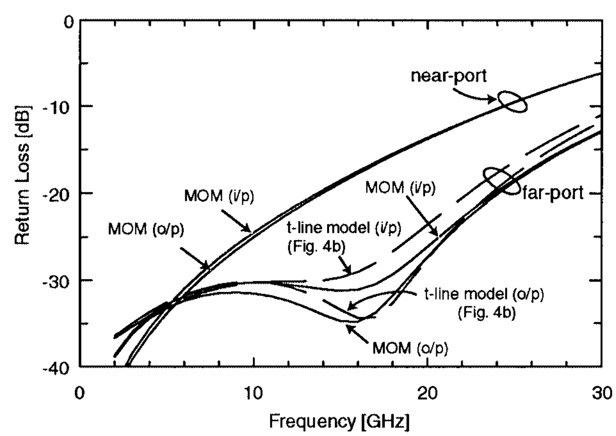

Fig. 4. Simulated input return loss (i/p) and output return loss (o/p) of the SP4T switch using ADS Momentum and circuit models.

B. Momentum and Circuit Simulations

The equivalent-circuit model in Fig. 3 provides a useful insight into the limitation of the SP4T circuit. However, it does not account for the coupling that exists between the lines in the SP4T switch and a full-wave analysis is needed (using ADS Momentum).[1] In the down-state position, the Rockwell Scientific MEMS series switch is represented by two strips of metal connecting the gaps. In the up-state position, the metal strips are ignored since they are 4-μm high and the circuit is simply a gap with a narrow metal strip connecting the dc pads at the left- and right-hand sides of the transmission line.

The Momentum simulations in Fig. 4 reveal that depending on which port is turned on, the SP4T switch exhibits either a “near-port” or the “far-port” return-loss response. This is

[1]*Advanced Design System 2001*, Agilent Technol., Santa Clara, CA, 2001.

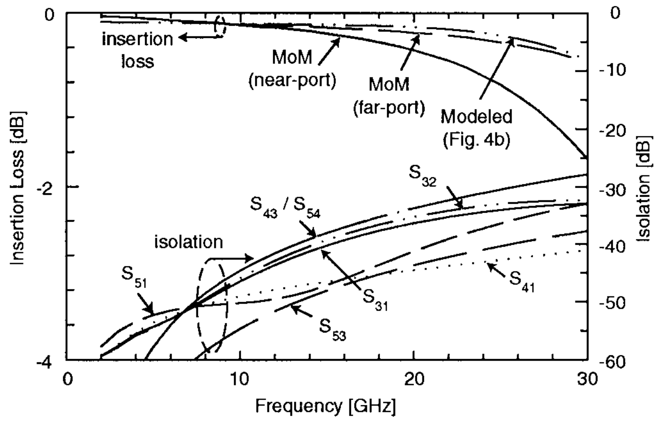

Fig. 5. Simulated insertion loss and isolation of the SP4T switch using ADS Momentum and transmission-line circuit model. The isolation is computed with $P1$–$P2$ connected (near port).

something that is not predicted by the equivalent-circuit model in Fig. 3(b). For the far-port return loss, the transmission-line model matches Momentum simulations very closely for both the input and output ports [see Fig. 4(a) and (b)]. However, the near-port return loss is not explained by the circuit model. It is thought that since the "near-port" is at an acute angle to the input port, there is some parasitic coupling that affects the input-output match. Hence, the near-port exhibits a narrower return-loss bandwidth than the far port in this design.

The simulated return loss of the SP4T switch is -20 dB up to 14 GHz, with an associated insertion loss of -0.21 dB at 14 GHz. At 10 GHz, the return loss is -25 dB and the insertion loss is -0.14 dB.

The dc pads and the associated via-holes (130-μm diameter) have little influence on the isolation response and may be ignored during the initial design, hence, speeding up the Momentum simulations considerably. They are included in the final Momentum simulation for completeness. The isolation is dominated by the gap distance between the input and output transmission lines and the SP4T switch has an isolation of approximately -45 dB at 10 GHz (Fig. 5).

C. Measured Performance of the SP4T Switch

The SP4T switches are fabricated using Rockwell Scientifics's proprietary fabrication process on 8-mil GaAs wafers [see Fig. 6(a)]. Insertion loss and isolation measurements for the four output paths of the standalone SP4T switch are available up to 3 GHz [see Fig. 6(b)]. It is seen that at least -45-dB isolation is obtained up to 3 GHz and the insertion loss is only -0.1 dB, corresponding to a switch resistance of approximately 1 Ω. The measured isolation is lower than the Momentum simulation in Fig. 5 because, in the simulation, the isolation is obtained with ports 1 and 2 connected, as in an actual application with a near-port connection (some signal is lost to port 2). Due to the port proximity in the standalone SP4T switch, such a condition obviously cannot be repeated during measurements and, therefore, the isolation is obtained with all switches in the up-state position.

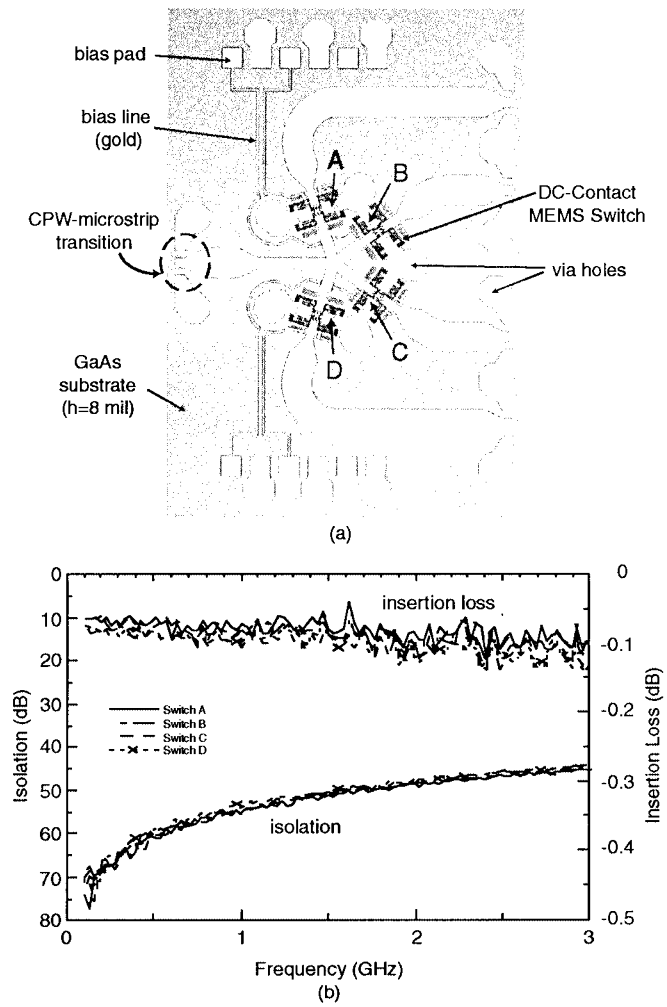

Fig. 6. (a) Photograph and (b) measured isolation and insertion loss of the SP4T switch (reference plane at the coplanar waveguide (CPW)–microstrip transition).

III. 2-bit Phase-Shifter Design

The 2-bit phase shifter is built on 8-mil (200 μm) GaAs substrates, using two SP4T switches (Fig. 7). The aim is to achieve an optimum design within 8–12 GHz with minimum insertion loss and size. The four delay lines required are 0°/90°/180°/270° in electrical length at 10 GHz. These four lines are placed between the two SP4T switches and the desired phase state is activated by turning on the MEMS switches connected to both ends of the particular delay line. There are only two switches in each path, in contrast to a conventional design based on SP2T switches, which has four switches. This means that, for switches with a resistance of 1 Ω, the SP4T design will have an insertion loss that is 0.2 dB better than similar designs with SP2T switches.

A. Design Considerations

The insertion loss of the phase shifter is mainly due to the metal and switch losses. Hence, in order to achieve a low-loss design, it is necessary to reduce the transmission-line length as much as possible. This is done by arranging the transmission lines to achieve the most compact design. Since every line must include a section equal to the reference line, the loss will be

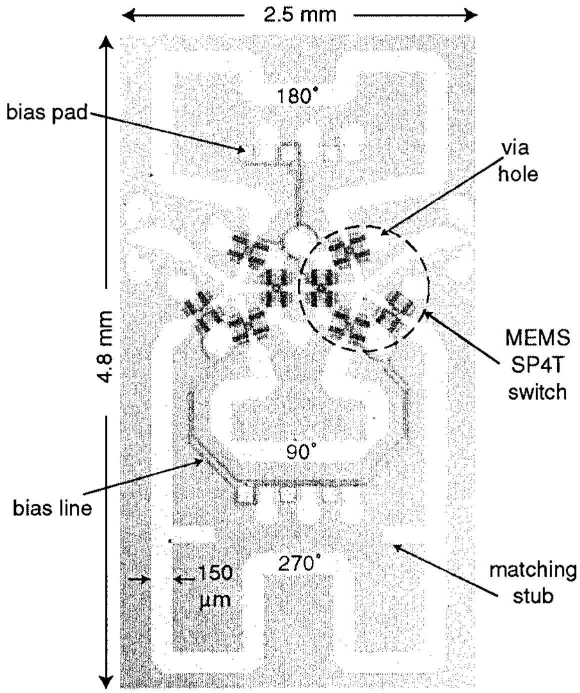

Fig. 7. Layout of the 2-bit SP4T phase shifter.

lowest if the reference line length is made almost zero. This is achieved by placing the two SP4T switches in a back-to-back configuration. All the delay lines are folded to reduce the circuit area using bends with a miter ratio $M = 0.3$, except the 90° lines, where two bends with $M = 0.7$ are used. This ratio is not the "optimized bend" that is often used in designs with bends. Rather, the miter ratio is chosen so that, with the geometrical layout, the best match is obtained with a complete Momentum simulation. An "optimized bend" would result in a better match for the delay lines themselves, but the overall phase shifter match will be degraded when the SP4Ts are inserted.

Due to the relatively high return loss of the near-port of the SP4T switch, a short pair of open stubs are needed along the 270° delay line to form a "T-match"-like configuration. The position and length of the stubs are chosen based on Momentum simulations. The stub dimensions are $W = 120$ μm and $L = 250$ μm, placed at 1270 μm from the beginning of the delay line. The simulated return loss of the 270° state is better than -20 dB from dc–14.5 GHz with the stubs and only -13 dB in the 8–12-GHz range without the stubs. The two short stubs together introduce an additional phase shift of 8° at 10 GHz, which is easily compensated by making the 270° line correspondingly shorter.

The delay lines in the phase shifter are packed as closely as possible in order to minimize the size. However, the coupling between the lines are kept ≤ -25 dB in order to prevent a distortion in the transmission phase of the lines. Fig. 8 shows the isolation (coupling) between the various delay lines in the final design, obtained using an eight-port simulation in Momentum. The isolation is better than -40 dB in most cases, with the exception of S_{73}. As would be expected, due to the two sections that are parallel to each other between the 90° and 270° lines, the coupling is higher than between other combination of lines. This limits the spacing between the 90°–270° lines.

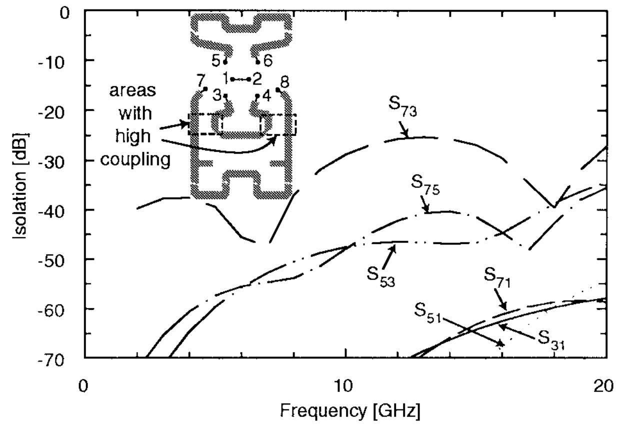

Fig. 8. Coupling (isolation) among the delay lines, as simulated by Momentum.

Switch biasing is done using very narrow (5 μm) gold bias lines and the dc ground is implemented using via-holes placed on either side of each MEMS switch. In the Rockwell Scientific switch, the bias lines and bias electrodes are completely decoupled from the RF contacts. Thus, the bias lines and bias electrodes have virtually no effects on the insertion loss of the phase shifter. This greatly simplifies circuit simulation and ensures the best RF performance in terms of insertion loss. Similar performance can be obtained using high-resistivity bias lines with at least 10 kΩ of bias resistance.

B. Momentum Simulation and Loss Breakdown

The design begins with the Momentum simulation of the near- and far-port configurations of the phase shifter. Since the bias electrodes and the dc vias are not expected to have a significant effect on the response, they may be omitted. However, they are included for completeness during the Momentum simulation. The delay-line network comprising four delay lines is then simulated as an eight-port network to include any coupling and the results are combined with the SP4T switch Momentum data in ADS to obtain the performance of the four phase states. The return loss, phase, and circuit size are then tuned simultaneously by repeating the above process.

The simulated return and insertion losses of the 2-bit phase shifter are shown in Fig. 9. The predicted return loss is better than -20 dB from dc–14.5 GHz. The insertion loss of the switch is -0.72 ± 0.25 dB over 8–12 GHz, assuming 1-Ω switch resistance (-0.17 dB for two switches). The loss contribution due to the switch resistance is given by

$$\text{Loss due to } R_s = 20\log_{10}\left(\frac{2Z_o}{2Z_o + R_s}\right) \quad (1)$$

which is frequency independent. The loss breakdown for each state is shown in Table I for $R_s = 1$ Ω and a gold metallization of 2 μm.

IV. 2-bit Phase-Shifter Measurements

A. Insertion and Return Losses

The measured and curve-fitted insertion loss of the phase shifter is shown in Fig. 9. In the curve-fitting simulation, the R_s value is adjusted so that the low-frequency loss matches the

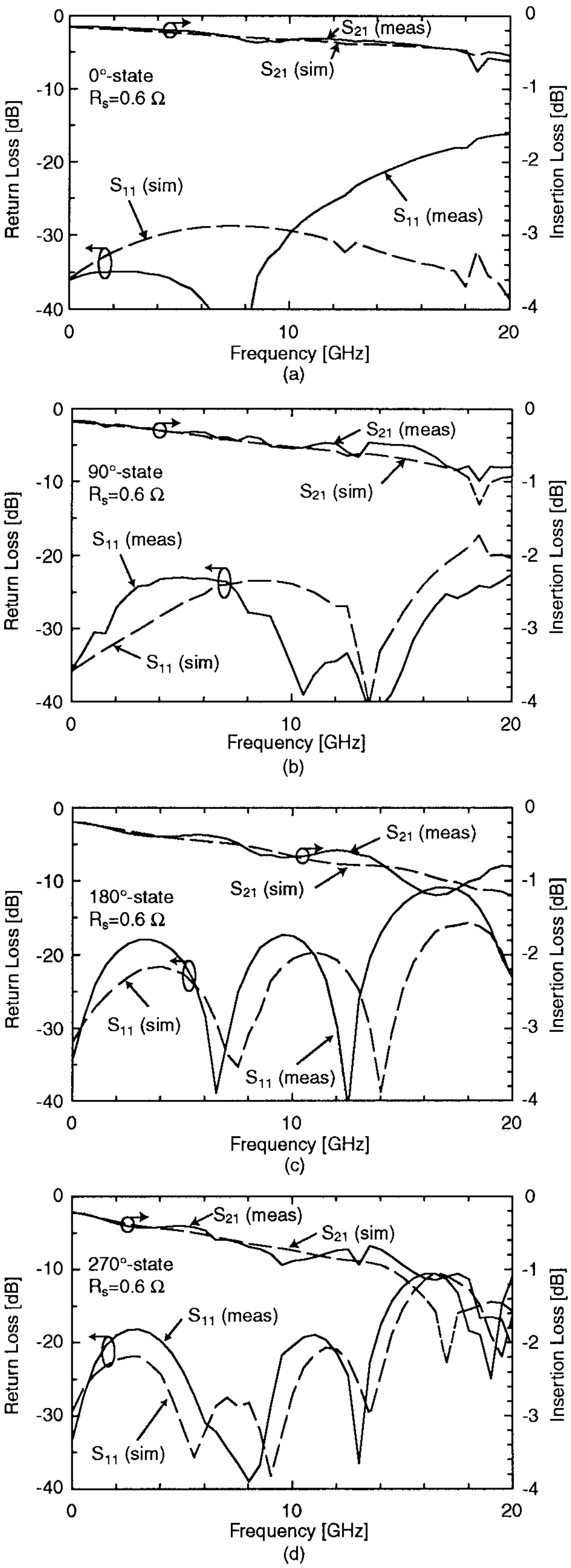

Fig. 9. Return- and insertion-loss measurement versus simulation for the 2-bit SP4T phase shifter. (a) 0°-state. (b) 90°-state. (c) 180°-state. (d) 270°-state. The measured insertion loss corresponds to an R_s of 0.6 Ω.

measured data. An $R_s = 0.6\ \Omega$ is obtained, indicating that the actual switch resistance is lower than the 1 Ω assumed in the initial simulations. The minimum and maximum measured losses within the 8–12-GHz design frequency range are −0.31 dB (0°, 11.5 GHz) and −0.94 dB (270°, 9.5 GHz), respectively, giving a measured loss of −0.62±0.31 dB over all phase states at 8–12 GHz. The associated return loss is better than −17.3 dB. The variation in insertion loss across the different phase states are inherent in designs using different lengths of delay lines to achieve the phase shift. The measured value of ±0.31 dB is comparable to other designs [2], [5].

TABLE I
SIMULATED (MOMENTUM) LOSS BREAKDOWN OF THE 2-BIT SP4T PHASE SHIFTER AT 10 GHz FOR THE DESIGN WITH MATCHING STUBS

Source of Loss	0°-state (dB)	90°-state (dB)	180°-state (dB)	270°-state (dB)
Switch (×2)*	−0.172	−0.172	−0.172	−0.172
Return loss	−0.006	−0.017	−0.039	−0.008
t-line (Au 2 μm)	−0.222	−0.411	−0.519	−0.630
Total Loss	−0.40	−0.60	−0.73	−0.81

* Assuming R_s=1 Ω.

The measured insertion loss is better than −1.2 dB from dc–18 GHz (average loss at 18 GHz is −0.85 dB) with a return loss of better than −10.5 dB. Momentum simulation indicates that there is a "dip" in the insertion-loss response at around 17 GHz due to off-path resonance [9]. This is also evident in the measured response, but it is shifted to around 20 GHz.

B. *Phase Accuracy and Group-Delay Response*

Fig. 10(a) shows the measured and simulated phase response of the 2-bit phase shifter. The differential time delays [see Fig. 10(b)], as computed by taking the negative gradient of the phase versus frequency response, are 0, 23.0, 49.0, and 72.8 ps, respectively, which correspond to a differential phase shift of 0°, 90.1°, 177.8°, and 272.0° at 10.25 GHz (phase accuracy of ±2°). The measured group-delay response is generally within ±5 ps from simulated values [see Fig. 10(b)]. The spikes in both the simulations and measurements may be due to the effect of off-path resonance [9].

V. 4-bit PHASE-SHIFTER DESIGN AND MEASUREMENT

The 4-bit phase shifter design uses four SP4T switches and comprises a 0°/90°/180°/270° "coarse-bit" section and a 0°/22.5°/45°/67.5° "fine-bit" section. The transmission lines for the coarse-bits are rerouted for a more compact layout. The coarse- and fine-bit sections are designed separately for the desired phase shift and with < -20-dB return loss at 8–12 GHz and their responses are combined in ADS. It is difficult to perform a Momentum simulation on the complete circuit as the mesh becomes too large when all of the eight delay lines are simulated together.

Using matching stubs as before, the simulated return loss is better than −15.5 dB within 8–12 GHz and the insertion loss at 10 GHz without R_s varies from −0.51 to −1.02 dB, giving an average loss of −0.76±0.25 dB. Since each path consists of four MEMS switches, there will be an additional loss of −0.34 dB if the switch resistance is 1 Ω, making the average loss −1.1 dB. The simulated average losses at 8 and 12 GHz with $R_s = 1\ \Omega$

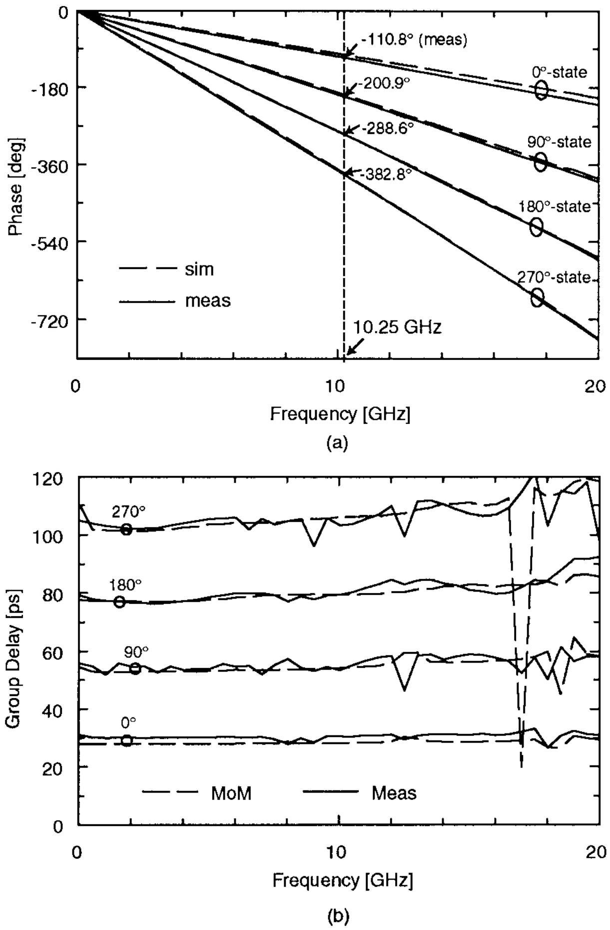

Fig. 10. (a) Measured versus simulated insertion phase for the 2-bit SP4T phase shifter. Simulations are performed with $R_s = 0.6\ \Omega$. (b) Group-delay measurement versus simulation for the 2-bit SP4T phase shifter.

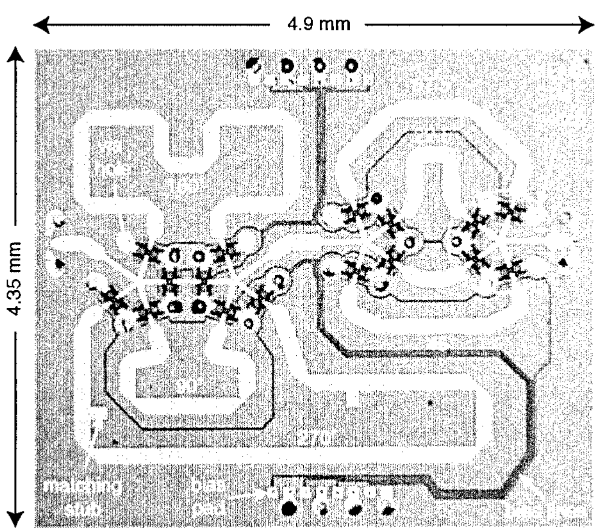

Fig. 11. Photograph of the 4-bit SP4T phase shifter.

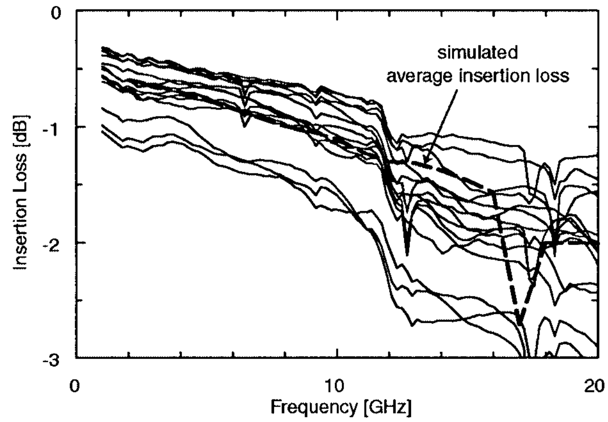

Fig. 12. Measured insertion loss and simulated average insertion loss ($R_s = 1\ \Omega$) of the 4-bit SP4T phase shifter.

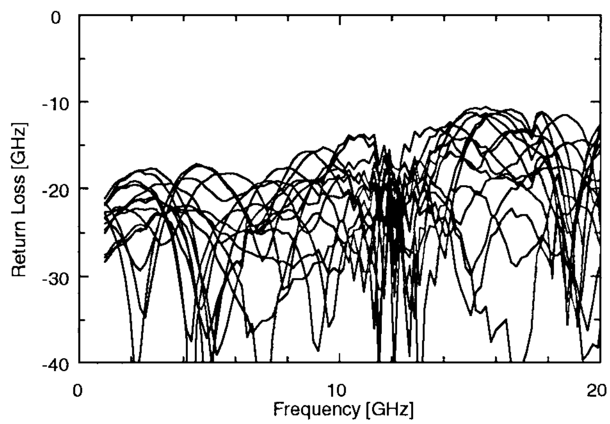

Fig. 13. Measured return loss of the 4-bit SP4T phase shifter.

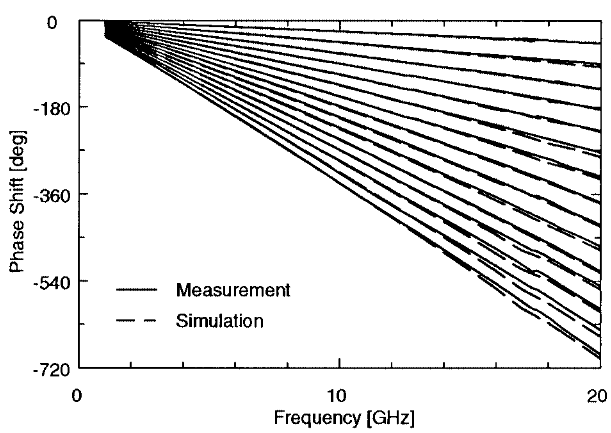

Fig. 14. Measured and simulated insertion phase of the 4-bit SP4T phase shifter.

are −0.99 dB and −1.30 dB, respectively. As before, the insertion loss response has a "dip" when the path includes the 270° delay line.

The 4-bit phase shifter is fabricated using the same Rockwell Scientific process and a photograph of the completed phase shifter is shown in Fig. 11. Measurements yield an average insertion loss of −1.0, −1.2, and −1.6 dB at 8, 10, and 12 GHz, respectively (Fig. 12). The losses of three of the 16 states are higher than expected due to the significantly higher switch resistance, which is evident from the increased low-frequency loss for these states. The switch resistance can be reduced in a future fabrication run and the average insertion loss is expected to improve by approximately 0.2 dB. For all phase states, the return loss is better than −14 dB within 8–12 GHz (Fig. 13) and the phase accuracy is within +2.3°, −0.9° at 9.97 GHz (Fig. 14).

VI. Conclusion

The insertion loss of MEMS phase shifters has been successfully reduced with SP4T MEMS switches. The 2- and 4-bit phase shifters designed using these switches achieved state-of-the-art insertion-loss performance and size. This study demonstrates that the RF performance of a complete MEMS phase shifter can be simulated accurately using a planar electromagnetic (EM) simulator. The 2- and 4-bit phase shifter presented above are a first-pass success and the measurements agreed very well with prediction. The bandwidth of the phase shifter can be further improved if the SP4T switch can be made smaller.

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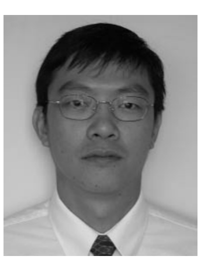

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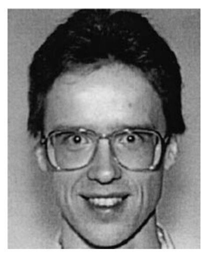
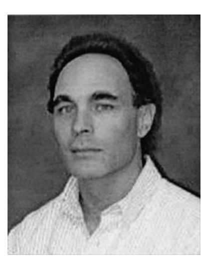
Upon graduation, he has studied and developed MEMS. His initial post-graduate position at Cornell University concerned the development and materials study of microresonators fabricated from single-crystal silicon. He subsequently joined the Army Research Laboratory, as a National Research Council Post-Doctoral Associate, during which time he developed device and fabrication technologies for military-relevant microsystems. Since 1996, he has been with Rockwell Scientific (RSC), Thousand Oaks, CA, where he focuses on RF MEMS devices, particularly on RSC's proprietary microrelay technology. This technical effort includes optimization of microrelay device to high-performance RF circuits. He has coauthored over 25 publications.



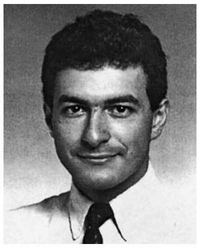
Jonathan B. Hacker (S'86–M'86) received the B.A.Sc. degree in electrical engineering from the University of British Columbia, Vancouver, BC, Canada, in 1986, and the M.S. and Ph.D. degrees in electrical engineering from the California Institute of Technology, Pasadena, in 1990 and 1994 respectively.

He is currently involved in research and development efforts in monolithic microwave integrated circuits (MMICs) including GaAs and InP HEMT and heterojunction bipolar transistor (HBT) devices, MMIC packaging, millimeter-wave spatial power amplifiers and multipliers, and phased-array antenna systems. He has performed pioneering research on spatial power-combining and frequency-multiplication techniques, as well as advanced MMIC devices integrating RF MEMS switches and HEMT structures. Prior to joining Rockwell Scientific, Thousand Oaks, CA, he was a Member of the Technical Staff with Bell Communications Research from 1993 to 1997, where he was involved in the development of advanced digital integrated circuits (IC) and multichannel modules (MCMs) for SONET and ATM applications.



Jeffrey F. DeNatale (M'01) received the B.S. M.S., and Ph.D. degrees in material science and engineering from the University of California at Davis, in 1980, 1983, and 1985, respectively.

He is currently the Manager of the MEMS Department, Rockwell Scientific, Thousand Oaks, CA. Since joining Rockwell Scientific, he has been involved with a broad spectrum of advanced research and development programs, including advanced optical thin-film materials, polycrystalline diamond thin films, high-temperature superconductors, and the first-ever demonstration of nonlinear thin films of the rare-earth nickelate family. Since 1997, he has led the MEMS efforts at Rockwell Scientific, directing a broad range of device activities. These include innovative projects in RF MEMS, industrial microsensors, optical MEMS, microassembly technologies and microthermal management devices. He has coauthored over 65 publications. He holds three U.S. patents with four pending.



Gabriel M. Rebeiz (S'86–M'88–SM'93–F'97) received the Ph.D. degree in electrical engineering from the California Institute of Technology, Pasadena, in 1988.

In September 1988, he joined the faculty of The University of Michigan at Ann Arbor, and was promoted to Full Professor in 1998. He held short visiting professorships with the Chalmers University of Technology, Göteborg, Sweden, Ecole Normale Superieur, Paris, France, and Tohoku University, Sendai, Japan. His research interests include applying micromachining techniques and MEMS for the development of novel components and subsystems for radars and wireless systems. He is also interested in Si/GaAs RF integrated circuit (RFIC) design for receiver applications, and in the development of planar antennas and microwave/millimeter-wave front-end electronics for communication systems, automotive collision-avoidance sensors, monopulse tracking systems, and phased arrays.

Prof. Rebeiz was the recipient of the 1991 National Science Foundation Presidential Young Investigator Award and the 1993 URSI International Isaac Koga Gold Medal Award for Outstanding International Research. He was also the recipient of the 1995 Research Excellence Award presented by The University of Michigan at Ann Arbor. Together with his students, he was the recipient of Best Student Paper Awards of the IEEE Microwave Theory and Techniques Society (IEEE MTT-S) (1992, 1999-1994), and the IEEE Antennas and Propagation Society (IEEE AP-S) (1992, 1995). He was also the recipient of the 1990 *Journées Int. de Nice sur les Antennes* (*JINA*) Best Paper Award, and the 1997 University of Michigan Electrical Engineering and Computer Science (EECS) Department Teaching Award. He was selected by his students as the 1997–1998 Eta Kappa Nu EECS Professor of the Year. He was also the recipient of the 1998 College of Engineering Teaching Award and the 1998 Amoco Foundation Teaching Award, given yearly to one faculty member of The University of Michigan at Ann Arbor for excellence in undergraduate teaching. He was the corecipient of the IEEE 2000 Microwave Prize for his work on MEMS phase shifters.